SIGNALLING METHOD AND APPARATUS

The present invention relates to a method and apparatus for transmitting and receiving digital electronic signals. It is particularly, but not exclusively, concerned with handling such signals in electrically noisy environments such as elevators.

Electronic signals are now being introduced into elevators, for a variety of reasons. It is an essential prerequisite of such systems that reliable methods of signalling are available to allow communication between the various electronic units. The capabilities which can be achieved in the electronics system will be held back if communication between units is slow, noisy or unreliable. Elevator systems present a particular difficulty in this respect as they are electrically noisy, with high power switching taking place nearby, and require signals to be transmitted over long distances.

The present invention seeks to provide a signalling system that is reliable in such an environment, which can be provided at relatively low cost, and which can be installed easily and without complexity.

The present invention therefore provides an electronic signalling system, comprising

a DC power source,

a power drain,

a cable interconnecting the source and drain, including atleast two cores,

a signal generator, and

a signal receiver;

the signal generator being adapted to modulate the power output of the source in dependence on the signal to be transmitted;

the signal receiver comprising a comparator adapted to compare the instantaneous power output of the source with a historical average power output thereby to detect the signal.

An embodiment of the present invention will now be described, by way of example, with reference to the accompanying Figures, in which;

Figure 1 is a schematic illustration of an elevator system;

Figure 2 shows a schematic circuit of the transmission unit;

Figure 3 shows a schematic circuit of the receiver unit; and

Figure 4 shows the modulated power output during a signal burst.

Since the introduction of electronic systems into the lift industry, means have been sought to enable electronic control and other subsidiary systems to have the following attributes:

(a) facilitate efficient installation;

(b) be cost effective in overall terms;

(c) operate efficiently;

(d) be robust in installation and operation;

(e) have high capability and exhibit advanced features.

The lift industry has to date met difficulty in meeting these requirements in a realistic and economic manner. It has proved unable, in many respects, to introduce "best practice" in difficult working environments and where electrical and electronics skills are in short supply.

The present invention seeks to provide a multi-purpose combined power and signalling system that meets the above requirements, particularly for lift systems. One application of this system provides the power distribution and signalling required for lift position and status indication by means of electronic visual and audio devices. The following example is described in the context of the lift industry but the principle could be applied usefully to many industrial applications.

A principal difficulty is the large number of wires previously required to connect position indicators. Typically one wire is required to enable the lift position to be indicated on position indicators; at best this was reduced to a binary or grey code equivalent. Signalling and power returns add still further difficulties. The overall result was complicated wiring and vulnerability to mis-operation due to non-ideal electrical factors, compounded by frequent failure due to incorrect installation.

Pre-existing industrial signalling solutions such as RS485 are insufficiently forgiving in installation and operation.

The combined power and signalling system described below enables both the transmission of power and signalling over one pair of wires. These wires can be ordinary 2-core mains wire rated to take the peak current of all the connected devices.

By way of context, Figure 1 shows a schematic illustration of an elevator system adopting the present invention. An elevator car 10 travels within an elevator shaft 12 between floors 14, 16, 18, etc. Each floor has the door such as that shown at 20, which corresponds to a door 22 within the elevator car 10. The doors 20 and 22 are suitably aligned when the elevator car 10 is correctly positioned. The elevator car 10 is suspended on an elevator cable 24, which is raised and lowered via a suitable electric motor (not shown). A cable 26 is suspended within the shaft and attaches to the elevator car 10 on a lower edge thereof. The cable 26 is sufficiently long to be suspended from the top of the shaft 12 and travel to the base thereof, before being connected to the elevator car at its lowest position via a short loop immediately below the elevator car 10. Thus, as the elevator car 10 ascends, the cable is pulled upwards with the car.

Each system includes a power supply encoder (one per system), located in the lift controller, and a receiving device (one or more per system), located at each landing and lift car.

The power supply encoder is shown in figure 2. Its function is to provide a source of unregulated, smoothed direct current power (V_{in}). An N-channel power mosfet 100 is then used to modulate this power supplied at 102 which is supplied to the receiving devices via output 104. From this, the connected receiving devices derive both power and signalling information.

The method of power modulation employed is 100% amplitude modulation. This requires that an N-channel power mosfet, optimised for 5 volt gate working, is switched completely on and off by the serial output of a microcontroller. The gate of this mosfet 100 is connected by resistor 106 between the serial input 108 and the gate thus allowing a small CR time constant to be imposed on the switching of the transistor, limiting the dv/dt of the amplitude modulation waveform and thereby reducing EMC propagation. By employing 100% amplitude modulation, power dissipation is minimised in the power mosfet device, allowing (e.g.) a TO220 package device to switch over 10 Amperes as the device spends a minimum of time in its linear region.

Short bursts of high-speed data ensure that the mean duty of the supplied voltage is greater than 90%, as during non-signalling periods (i.e. most of the time) 100% duty is supplied.

A discharge resistor 110 allows the output voltage to return to V_{in} between bursts.

Thus, two outputs are provided, in the form of a switched negative 104 and an unswitched output of V_{in} at 112.

There are a number of types of receiving devices, such as digital displays and speech units. Each incorporates a demodulator incorporating a means for (i) storing energy during power discontinuity (signalling bursts); (ii) demodulating the received modulated power; (iii) line discharge during modulation. Beyond these units, the nature of the receiving device is essentially irrelevant to the invention.

Storing of energy during power discontinuity (i.e. signalling bursts) is achieved by charging a capacitor 200 (C_x) when power is present on the input lines 202, 204. This capacitor is prevented from discharge, by routing the charging path via a power diode 206 (D_c). Thus when the received voltage VR is less than that on the capacitor there is no external current flow. The charge on the capacitor 200 (C_x) provides a power output at 208, 200 for the device during signalling bursts and the capacitor is sized accordingly.

Demodulation of the incoming power to each receiving device is achieved by means of a comparator 212. This comparator is connected so that one input 214 is derived from the capacitor C_x, thus establishing itself at voltage proportional to the mean incoming voltage, whilst the other input 216 of the comparator is derived from the incoming signal prior to the charging diode (D_c), and reflects the instantaneous voltage on the line. A small amount of hysteresis is established to minimise the effect of noise. The output 218 (V_s) of the comparator 212 is passed to the serial data input of the receiving device microcontroller, which in turn decodes the data present on the incoming modulated power signal.

The inputs 214, 216 to the comparator are in fact set at a simple fraction of the received voltage V_R and the output voltage V_s by way of potentiometer bridges. Thus, the input 216 detects the received voltage V_R after division by resistors 222 and 224 arranged as a potentiometer across V_R. Likewise, the input 214 detects V_s by way of resistors 226 and 228 arranged as a potentiometer across V_s. The resistors 222, 224, 226 and 228 can be selected at suitably high values to limit the current drawn from capacitor 200.

When the encoder power mosfet device is switched off during signalling bursts, resistors (Rd) 110 and 220 at each node provide a means of discharging the

line capacitance, enabling a suitable waveform to be presented to the demodulation circuitry. These resistors (Rd) 100 and 200 are chosen to enable unit length discharge of the line to take place during a power discontinuity. These resistors are chosen to optimise the discharge time, thus reducing EMC emissions whilst allowing adequate signalling speed.

Figure 4 shows the wave form at 104 of Figure 2 during a signalling burst. It will be appreciated that at times when no signal is being passed, 104 will provide a zero voltage reference as compared to the modulated voltage at 112. During signal bursts, mosfet 100 becomes non-conducting and the voltage at 104 rises to the regulated input voltage. Thus, during a signal period such as that shown at 300, the voltage briefly rises to V_{in} before dropping back to substantially zero at 302.

The pulses can be of any width or pattern of widths as required by the signalling method chosen.

Whilst a voltage pulse is taking place, the voltage on the capacitor 200 at the receiving unit will of course slowly decline. This is indicated by the dotted line 304 on figure 4, showing that even allowing for reasonable current consumption by the receiving unit, an adequate voltage difference is maintained to allow the comparator 212 to detect a signal, provided that the capacitor 200 is an adequate rating and the pulses are sufficiently short.

For the sake of completeness, the detailed specifications of the parts appearing in Figures 2 and 3 are given below. However, it is to be understood that the invention is not limited to the specific values presented herewith by way of example:

Figure 2 - Encoder Power Switching Circuit

100

Part 100 IRLZ24 is an n-channel power mosfet optimised for working at 5 Volt TTL gate voltage. It is able to switch DC currents in excess of 12 amperes at voltages greater than 50 Volts.

102

Point 102 is the power supply input, which for this application is a smoothed but unregulated DC voltage between 9 and 40 Volts DC.

104

Point 104 is connected to the drain of the power mosfet (100) and is the switched negative line of the 2-wire power/signalling line. When the power mosfet device (100) is switched on and current flows this point is substantially at 0 Volts DC and hence maximum voltage appears across the load points 112 and 104. When power mosfet device (100) is switched off during periods of signalling during which gate voltage of device 100 is at 0 Volts and hence switched off, voltage at point 104 rises to V_{in} (102) supply voltage.

106

Component 106 is a 10K resistor which is series with the TTL 5 Volt level issued by the microcontroller serial data output and the gate of power mosfet (100). The purpose of this component is to limit the charge and discharge rise and fall time of the gate. This limits the turn on and turn off rate of change of the mosfet device (100) so as to limit EMC emissions.

108

Point 108 is the serial TTL level output of the microcontroller. In this application the data rate is limited to 9600 bits per second. During signalling bursts this voltage is switched between 0 and 5 Volts, whilst between signalling bursts this point remains at 5 Volts.

110

Component 110 (R_q) is a resistor whose value is typically 1K ohms and rated at 1 Watt. The purpose of this resistor is to discharge the line when mosfet (100) is switched off, so that the rate of change of voltage decay between points 112 and 104 is able to follow more closely that of the voltage decay of the gate of mosfet (100).

112

Point 112 is the positive (non-switched) line of the 2-wire system. This point is always at supply potential (V_{in} point 102).

Figure 3 - Power Separation and Signalling Detector Circuit

200

Component 200 is an electrolytic capacitor of 33uF rated at 40V. The purpose of this device is to charge capacitor 200 from line via diode (206) when voltage across the 2-wire signalling lines is greater than that across capacitor 200. This provides power continuity during signalling bursts, when instantaneous voltages fall to 0 Volts.

202

Point 202 is the negative 0-Volt, switched input of the receiving device to

powered and signalled over the 2-wire signalling system. Between signalling bursts this point is at 0 Volts, when full supply voltage is being supplied to line from the encoder. During signalling bursts the instantaneous voltages equals that of 204 when encoder power device (100) is switched off.

204

Point 204 is the positive (un-switched) supply input of the receiving device connected to the 2-wire signalling.

206

Device 206 is a 1N4005 power diode rated at 1 Amp. Current flows when the potential across input points 202 and 204 exceeds that across capacitor 200 + 0.7 Volts. When capacitor 200 is fully charged the current passing through diode 206 is the instantaneous current required by the supplied receiving device. During periods of signalling bursts diode 206 prevents capacitor 200 discharging to line.

208

Point 208 is the 0 Volt internal connection to the receiving node. It is the same potential as point 202 and at a potential of - V_{out} with respect to point 210.

210

Point 210 (V_{out}) is the positive internal connection to the receiving node. It is at potential V_{out} which is the instantaneous value of the voltage across device 200, capacitor C_x, with respect to point 208.

212

Device 212 is a single supply comparator that compares voltages 214 and

216, depending on the relative levels present at these points outputs a voltage of either 0 or 5 Volts at 218.

214

Point 214 is the inverted input to the comparator 212. This point is connected to the potential divided 226 and 228 and is set at a potential determined by the ratio of the 2 resistors 226 and 228 and is set at a potential determined by the ratio of the 2 resistors 226 and 228 and the instantaneous 210 (V_s). 214 thus represents a proportion of the internal supply voltage.

216

Point 216 is the non-inverted input to the comparator 212. This point is connected to the potential divider 222 and 224 and is set at a potential determined by the ratio of the two resistors 222 and 224 and the instantaneous voltage 204. 216 thus represents a proportion of the instantaneous voltage at the input of the receiving node.

218

Point 218 is the output of comparator 212. This output voltage is the detected logic level serial data, which is connected to the serial data input of the microcontroller.

220

Device 220 is a resistor of value 2K7 ohms. This resistor contributes the function of discharging the capacitance of the 2-wire power/signalling system.

222

Device 222 is a resistor of value 1K ohms and is part of the potential divider

that derives voltage 216.

224

Device 224 is a resistor of value 10K ohms and is part of the potential divider that derives voltage 216.

226

Device 226 is a resistor of value 470 ohms and is part of the potential divider that derives voltage 214.

300

Point 300 represents part of a signalling burst at the input of one of the signal receiving devices. At this point in time there is 0 Volts across the input terminals 202 and 204 as the encoder/signal generator used to modulate and supply power to line has been turned off and hence the voltage is at supply voltage potential.

302

Point 302 represents part of a signalling burst at the input of one of the signal receiving devices. At this point in time there is V_s (Supply Voltage) across the input terminals 202 and 204 as the encoder/signal generator used to modulate and supply power to line has been turned on and hence the voltage is at 0 Volts supply potential.

Figure 4

Figure 4 represents part of a signalling burst at the input of one of the signal receiving devices (up to 64) across input terminals 202 and 204. Between

signalling bursts this voltage is at maximum supply voltage minus any voltage drops due to line resistance.

It will of course be appreciated that the above described embodiment is purely illustrative of the present invention.